

Docket No.: 42478-6200

RESPONSE UNDER 37 CFR SECTION 1.116
EXPEDITED PROCEDURE - GROUP 2857**FULL VERSION OF PENDING CLAIMS**

1 1. (Previously Presented): A multilayer board on whose outside layer, one or more
2 circuit components are mounted, the multilayer board comprising:

3 a signal line requiring tamper-resistance, the signal line being connected to a
4 predetermined component among the one or more circuit components and including: (a) a
5 conductive trace and (b) a conductive via that passes through layers of the multilayer board,
6 wherein

7 the conductive trace and an end of the conductive via existing on the outside layer
8 of the multilayer board are placed only under the predetermined component, and not on the other
9 area of the outside layer.

1 2. (Original): The multilayer board of Claim 1, wherein
2 the signal line further includes a conductive trace on an inner layer that is
3 sandwiched between sheets of foil and/or circuit components placed on layers above and below
4 the inner layer so that the sheets of foil and/or circuit components hide the conductive trace on
5 the inner layer when viewed from above or below.

1 3. (Original): The multilayer board of Claim 2, wherein
2 the sheets of foil placed on the layers that are outside the inner layer are
3 connected to either a ground or a power source.

1 4. (Original): The multilayer board of Claim 3, wherein
2 the conductive trace on the outside layer is further covered by a circuit component
3 on another outside layer when viewed from above or below.

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1 5. (Original): The multilayer board of Claim 2, wherein
2 the signal line requiring tamper-resistance is either a signal line that is input to an
3 encryption unit or a signal line that is output from a decryption unit.

1 6. (Previously Presented): A multilayer board on whose outside layer, one or more
2 circuit components are mounted, the multilayer board comprising:
3 a certain signal line that is connected to a predetermined component among the
4 one or more circuit components and includes (a) a conductive trace and (b) a conductive via that
5 passes through layers of the multilayer board, wherein
6 the conductive trace and an end of the conductive via existing on the outside layer
7 of the multilayer board are placed only under the predetermined component, and not on the other
8 area of the outside layer,
9 the certain signal line further includes a conductive trace on an inner layer of the
10 multilayer board, the conductive trace being sandwiched between sheets of foil and/ or circuit
11 components placed on layers above and below the inner layer so that the sheets of foil and/or the
12 predetermined component hide the conductive trace on the inner layer when viewed from above
13 or below, and
14 the certain signal line is either a data line or an address line.

1 7-29. (Cancelled)

1 30. (Currently Amended): A tamper-resistant multilayer board for transfer of pixel
2 data to be encrypted comprising:
3 a board member having a plurality of layers and one or more components
4 mounted thereon;

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5 a reception/decryption unit mounted on the board member;

6 an output interface unit mounted on the board member and operatively connected

7 to the reception/decryption unit; and

8 a conductive path operatively designed for interconnecting the reception/

9 decryption unit and the output interface unit and positioned adjacent an interior layer surface for

10 a first portion of the conductive path and positioned only under the reception/decryption unit

11 and/or the output interface unit ~~[[only]]~~ for ~~the remainder~~ a second portion of the conductive path

12 on an outside layer of the multilayer board to prevent direct access to the second portion of the

13 conductive path from the exterior of the board member.